

Multi-image displays

Control rooms are turning toward multi-image displays to replace traditional monitoring.

BY AUGUSTO VILLASEÑOR

In the early 2000s, companies that provide multi-image display technology started to offer several new improved variants to the broadcast industry. Their primary targets were control rooms and presentation suites in master control facilities for the display of multiple windows of video, audio and data on unified screen monitors. Previously, because of concern about reliability and unstable pictures, many broadcast engineers shunned the idea of multi-image displays.

But, the new generation of high-speed Field-Programmable Gate Array (FPGA) logic solved most of those problems. Instead of many small CRT monitors populating a control room, the sight of plasmas and LCDs are becoming a de facto standard for displaying audio, video and data signals in broadcast centers.

Processing

Multi-image display processing envisions the entire area of the screen as a graphical canvas. This canvas is the design working area where windows can be created to tie the audio/video images coming as signal sources to the processor.

Figure 1 shows the logical representation of how a screen is being treated by a display processor. The canvas size is equivalent to the display screen's total resolution and congruent to the processor's supported output. Making a window on the canvas pertains to creating one logical video monitor. The size and shape of it determines the proportionate image to be rendered and presented.

It is imperative that the screen's — or combination of screens, such as LCD, plasmas, projection cubes, etc. — native resolution must be able

to support the highest capacity of the processor's output. When a signal has a resolution that exceeds the display panel's supported resolution range, a simplified image will be presented. For example, if the processor supports up to an SXGA output, the display screen must at least be able to display 1280 x 1024 resolution within its range. Otherwise, the screen canvas will be a mismatch of the screen representation. Some display screens will not allow presentation of out-of-range resolution.

As illustrated in Figure 1, the processor drives the single screen with multiple windows created on the canvas. In fact, given that there are multiple windows sharing the XGA (1024 x 768) canvas, the resulting window occupies less lines and pixels on the display screen. The processor retains the aspect ratio of the original signal,

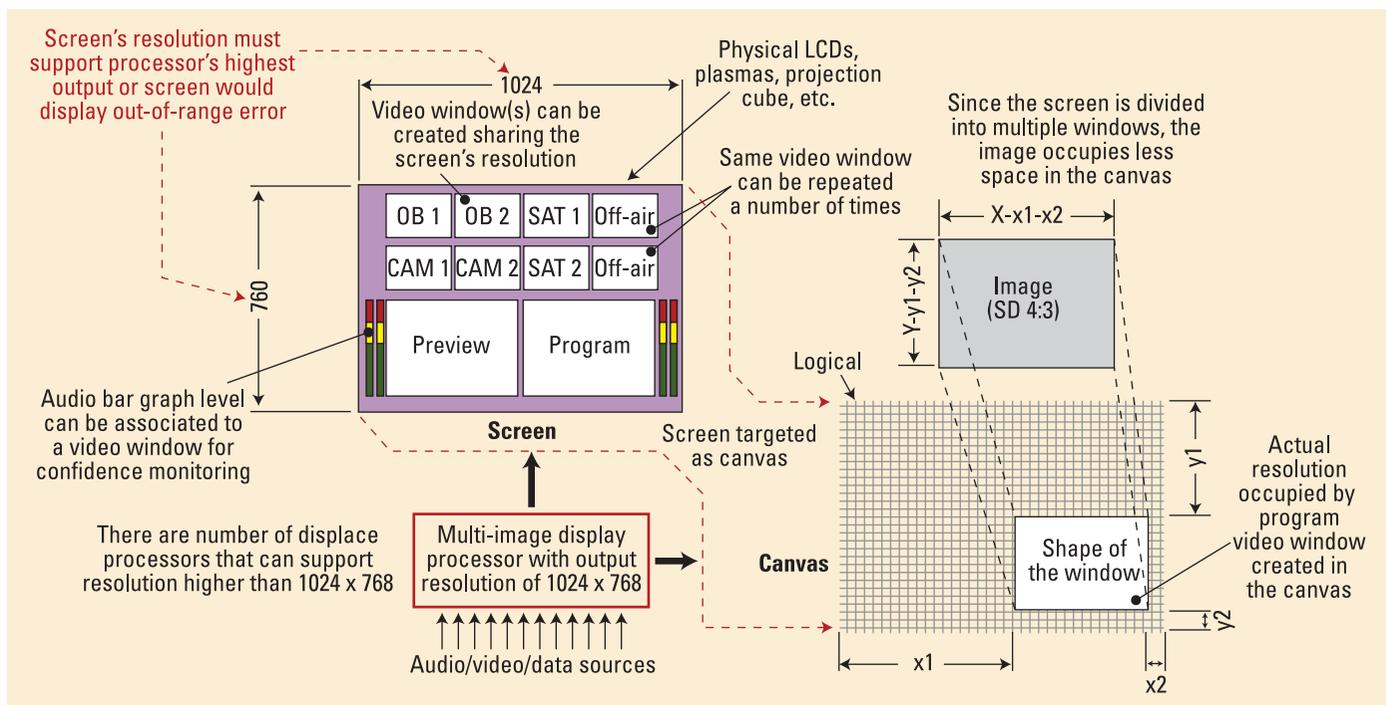


Figure 1. Working canvas area equivalent to the screen XGA resolution with multiple windows created to present audio/video sources

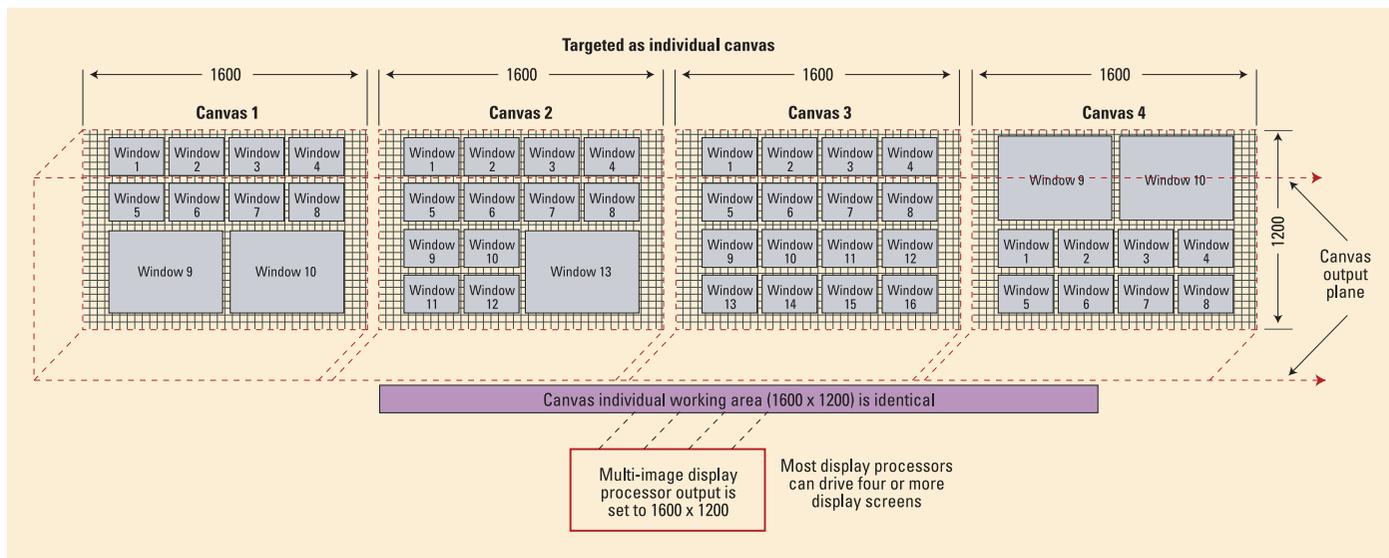


Figure 2. Single processor driving four independent display screens

but the processor will deliver the image based on the available graphical space shaped. When the signal program window is presented on the screen, the actual canvas it occupies gives the resolution:

$$X=1024-x1-x2$$

$$Y=1024-y1-y2$$

The SD signal corresponds to the X- and Y-axis of the canvas. If X starts from line 472 and terminates on line 15 at the bottom, then it occupies 282 lines. Knowing the Y value, then X can be computed as 376, which results in a picture ratio of 1.33. If the program video is encoded at 704 x 480, the processor presents it on a simplified 376 x 282 form. The artifacts of less resolution are concealed to the user because the image space rendered is a small window (of moving images), proportional to the signal (aspect ratio and refresh rate) and occupying less than the real canvas area (required for full-screen display).

Typically, a processor supports one canvas per screen. In a linear output configuration, the screens are autonomous of each other. The processor can conceive the target screens as a multiple of solo canvases. (See Figure 2.) It represents four independent canvases driven by a single processor. Windows drawn in one canvas area will not affect the other. The highest 1600 x 1200 canvas-working area is maintained along individual canvases, assuming

the display screens can carry on UXGA depth. Different symmetrical shapes can be designed on an individual canvas for the same source(s) because all canvases have access to the processors' frame inputs. When additional screens are added, it can be envisioned as another canvas space.

Most multi-image display processors support multiple outputs. Although each output is physically separate, they can be threaded as one logical output in the processor. Figure 3 depicts the higher degree of design canvas to operate on multiple screens integrated as one logical presentation

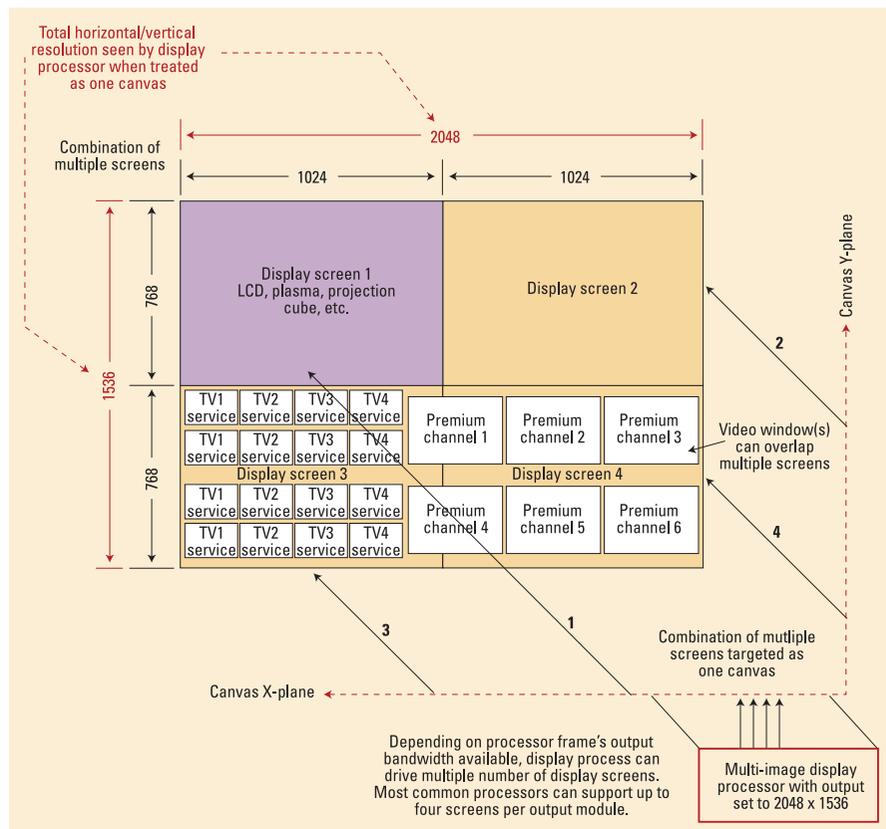


Figure 3. A 2 x 2 display block forms one unified display conceived as one target canvas.

display. Multiple display panels are unified to form a larger design working area. This 2 x 2 screen arrangement results in wider horizontal and vertical depth. Note that the processor pooled the horizontal and vertical axis resolution to obtain the total of 2048 x 1536 into one array (doubling the XGA). The Y-axis plane (768+768) corresponds to the increasing number of screens vertically (for warp orientation), while the H-axis relates to extra panoramic view (1024+1024).

The resulting rectangular area is the design canvas working space. For

face on their auto-sensing wideband input. (See Figure 4.) The processor uses specialized hardware to detect a bit pattern known as Timing Reference Signal (TRS) framing to recognize the SDI data stream. Framing is the process determining where in a serial data stream characters begin and end. For SDI, the TRS consists of a three-character sequence of 0x3FFh, 0x3FFh and 0x000h in 10-bit hex, respectively. TRS for HD-SDI has embedded additional 0x000h, 0x000h and 0x000h for a six-word sequence. This TRS can still have SD-SDI TRS

SD signal, regardless of analog or digital in 4:3 modes. Any windows created for SD occupies 1.33 aspect when presented on-screen. For HD, the default panel is always 16:9 types. It is possible to create an unsymmetrical aspect ratio in the canvas. However, the result may be a misrepresentation of the actual proportion because the processor will attempt to fill the window with a picture image when it is formed.

For audio inputs, the multi-image processor can accept SDI embedded audio as inputs. The input module extracts SDI's ancillary blanking lines

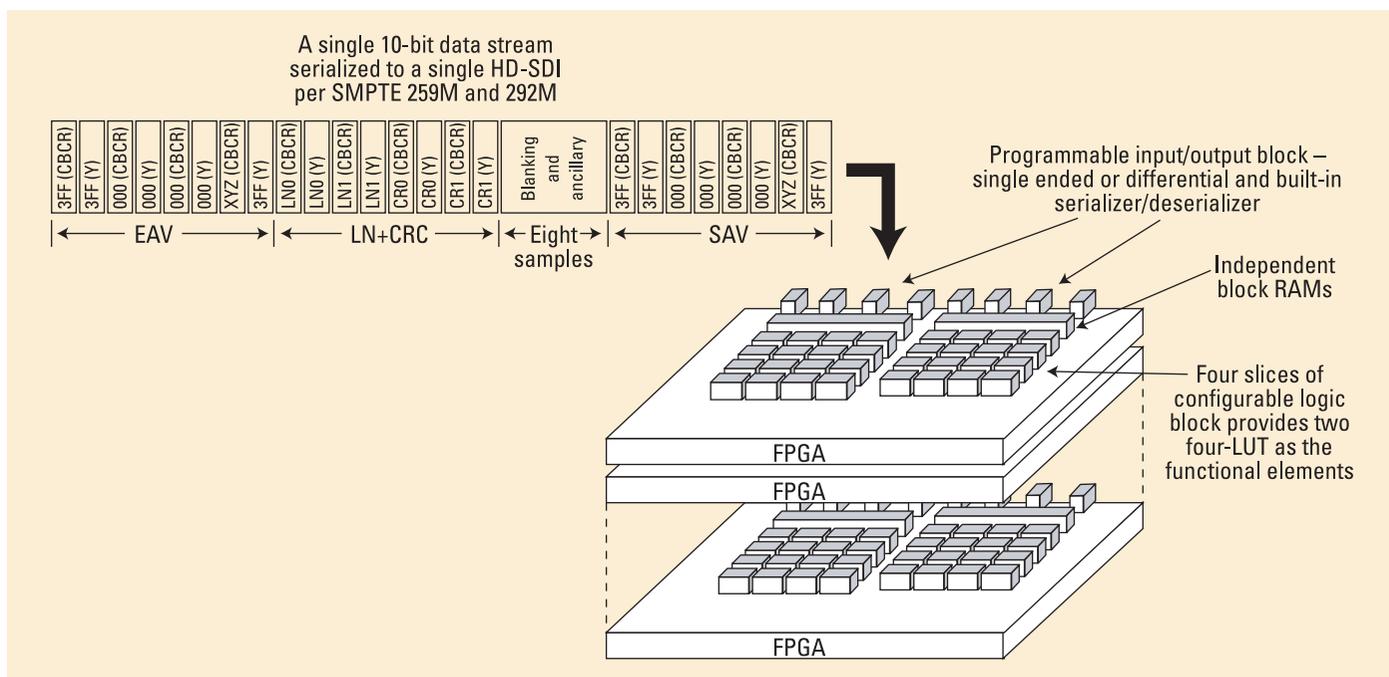


Figure 4. Multi-image processor using Field-Programmable Gate Arrays

this setting, a single picture window can overlap on multiple screens. The drawing canvas assumed (logically) that the spaces allocated for windows creation are presented on one display screen. In combining multiple screens to form arrays, the processor resolution oftentimes has a limitation of a maximum logical space (canvas size) it can support. It is necessary to check the best resolution the processor output can handle before forming screen arrays.

Sources

Multi-image processors can support the SD/HD multiformat inter-

in the same order, as it would occur in HD-SDI. Hence, video sources can be processed by auto-detecting character boundaries based on pattern 0x3FFh, 0x000h, 0x000h, 0x000h, 0x000h and 0x000h that is embedded between the EAV and SAV of the horizontal line. The processor's wideband input module flags the character arrangements to identify the source.

Differentiating between SD and HD sources in the canvas requires the processor to determine aspect ratios appropriately. The processor logical canvas has predefined templates or patterns available for both SD and HD. Normally, the processor treats the

for audio data. For discrete analog sources such as analog stereos and AES digital audio, processors have daughter cards to associate audio received to any video input. Up to eight channels of audio can be married to any sources, and a bar graph for level metering can be made on the canvas.

Presentation

Multi-image display technology offers the highest level of signal presentation flexibility. The number of windows that can be created on the canvas depends on the available space. Once the target canvas is ready, windows of video, audio bar graph and other static

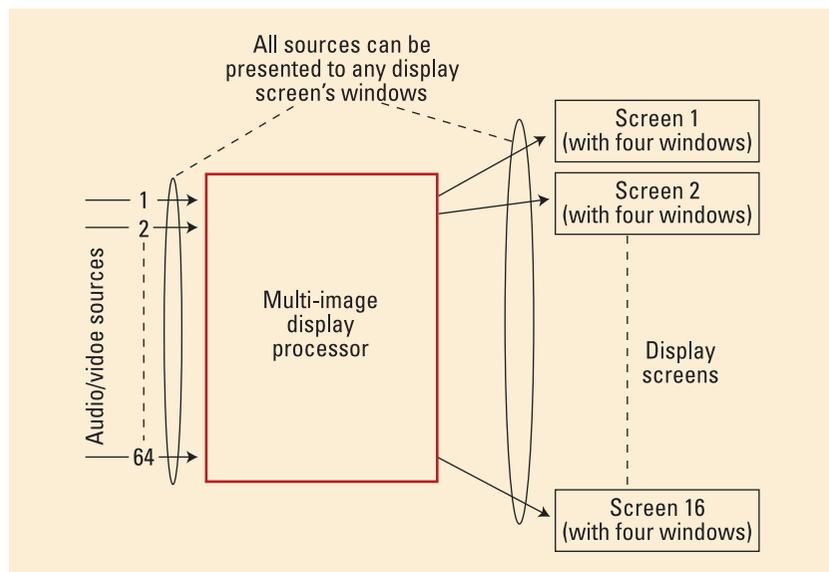


Figure 5. Unified architecture

text metadata, such as channel name labels and UMDs, can be inserted.

Dynamic metadata such as Closed Caption (CC), eXtended Data Service (XDS), Teletext service (for PAL), source ID, program rating and audio types can be automatically detected and presented. Any input sources coming into the processor can be assigned to any window created. The processor can display HD, SD or analog inputs any number of times, in any size, across multiple displays of supported resolution and orientation.

Alarms

For confidence monitoring ap-

plications where signal presence is a must to maintain service level, multi-image displays provide the necessary tools to monitor and check baseband status at all times. Processors have the ability to recognize alarms from individual input sources. They use loss of carrier in the SDI data stream to indicate loss of video.

For CC fault detection, the processor buffer lines 21 and 22 for loss of CC waveform to report CC error. Audio silence was based on the lowest input threshold level set (say -80dB) to trigger loss of audio alarm. Other alarm detections are EDH errors, active picture levels, frozen video, black

video, motion detection, video format detection, loss of audio channels, mono audio detection, phase reversal detection, audio too loud, audio too quiet, loss of CC channels, loss of text channels, loss of program rating, source program ID missing and more.

Although multi-image processors have the capability to detect indication of faults at system level and provide a snapshot of the status of the signal by notification, they do not lend themselves to analyzing the signal problem in detail. It is a common misconception to treat multi-image processors as test-and-measurement devices.

Topologies

The following are sample deployment architectures for multi-image display processors. First is the centralized topology, where all input sources are processed and displayed using a single frame. (See Figure 5.) The frame can be fitted with minimal input modules to handle the required number of sources initially. To accommodate more sources, the frame is populated with additional modules to the maximum capacity. When adding a display becomes necessary, an output module can be inserted into the frame to drive more screens.

One important feature of this architecture is that all input sources can be

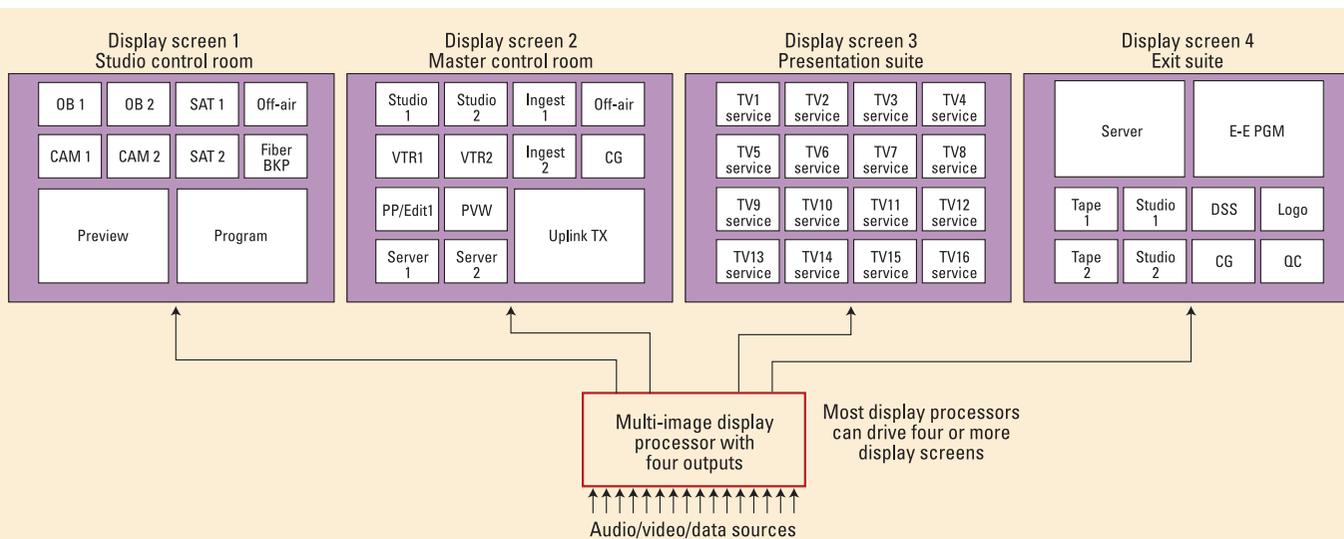


Figure 6. Multi-room monitoring on a single processor

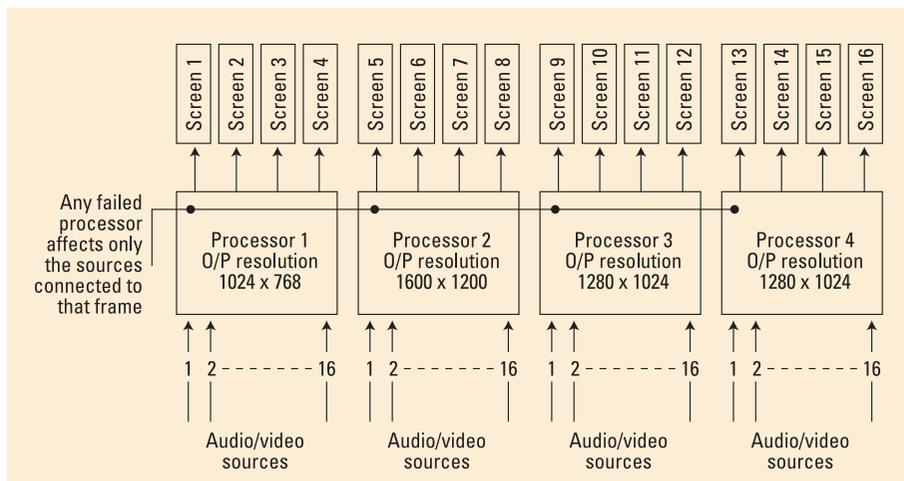


Figure 7. Autonomous architecture

assigned to any output screens. This setting also simplifies deployment and is fairly easy to manage. All cabling infrastructure terminates in one place. An added benefit of this scheme is related to the question of screen reliability. Display screens can fail without affecting the operation of the remaining screens. This allows the operator to use the remaining displays while a faulty screen is being repaired or replaced. This is often preferred for multiroom applications, where monitoring per functional area is required. (See Figure 6 on page 72.)

A single processor is good for a small implementation where the number of sources is static and expansion is fixed to the maximum slot capacity of the frame. Once the maximum modules in the frame are inserted, there will be no more room for any future increase

of input sources or output screens. Another problem is that having one frame means a single point of failure. In the event of a failure, the entire monitor is completely down.

Distributed architecture employing multiple processors to drive independent multiple screens provides high reliability. A failed processor does not affect other frames in the system. Each processor acts autonomously, thus providing complete isolation of screens connected to it. Distributed processing can operate without resolution dependencies to other screens in the system because their drawing canvases can be set individually per processor. (See Figure 7.) Distributed systems can increase input sources and screens without interfering with the other processors' operation.

One major disadvantage of a distrib-

uted topology is the source assignment. Because they are not linked together, sources from one processor cannot be assigned to the other, thus preventing the screen access to those sources.

In designing for full-size NOC monitoring, the hybrid scheme architecture of linking multi-image processors is best suited for more display screens and more input sources, yet allows an easy to understand method of expansion. The hybrid follows the X and Y plane to allow expansion of both input (sources) and outputs (screens).

Figure 8 illustrates an example of a hybrid system married to support an unlimited number of sources, and capable of expanding display sources as the need arises. The processors in the vertical column thread can be expanded to an additional number of frames to accommodate more input without increasing the screen panels. Extending the horizontal plane increases the number of displays that can be driven if more screens are desired to render larger window images.

The cascaded-tree has the highest system reliability. For monitoring that requires more input sources, a multi-image processor can be operated in cascaded manner. In this scenario, there will be more input sources available for expansion without increasing the number of screens. All sources can be assigned to any

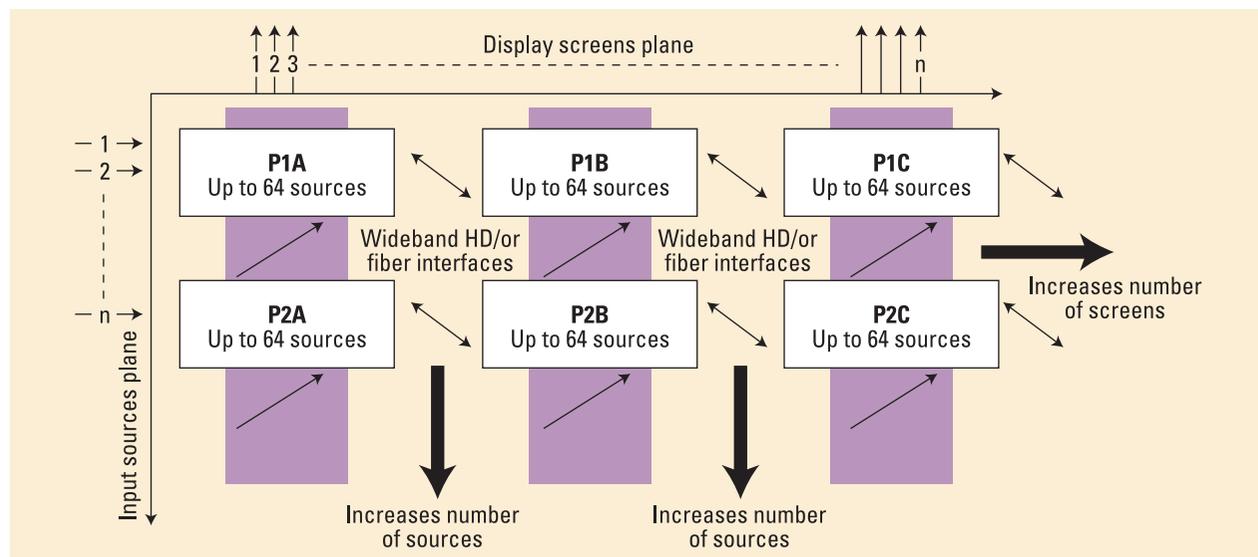


Figure 8. Hybrid architecture

screens. Any failed processor, other than the primary and backup, affects only the signal sources physically connected to that frame.

Figure 9 shows an example of multi-processor design in cascaded-tree fashion. The frame P1A and P1B are allocated as output processors in 1:1 redundancy. All display panels are connected to these two frames. P2, P3, P4 and P5 are both designated as in-

taken into consideration. First, it starts with outlining the functional requirements. Determine the locations, rooms and areas where monitoring will be needed. Decide the type of monitoring required on each functional area.

Second, differentiate input sources and formats. Segregate SD and HD signals sources respectively. Although the image processor is capable of accepting both, it is helpful

image display over conventional monitors is that it has proven value-added features such as alarm notifications and faults triggering using the Simple Network Management Protocol (SNMP) interface. Most display processors' control software applications can report to a higher-level SNMP manager or third-party Network Management Systems (NMS), thereby improving overall monitor-

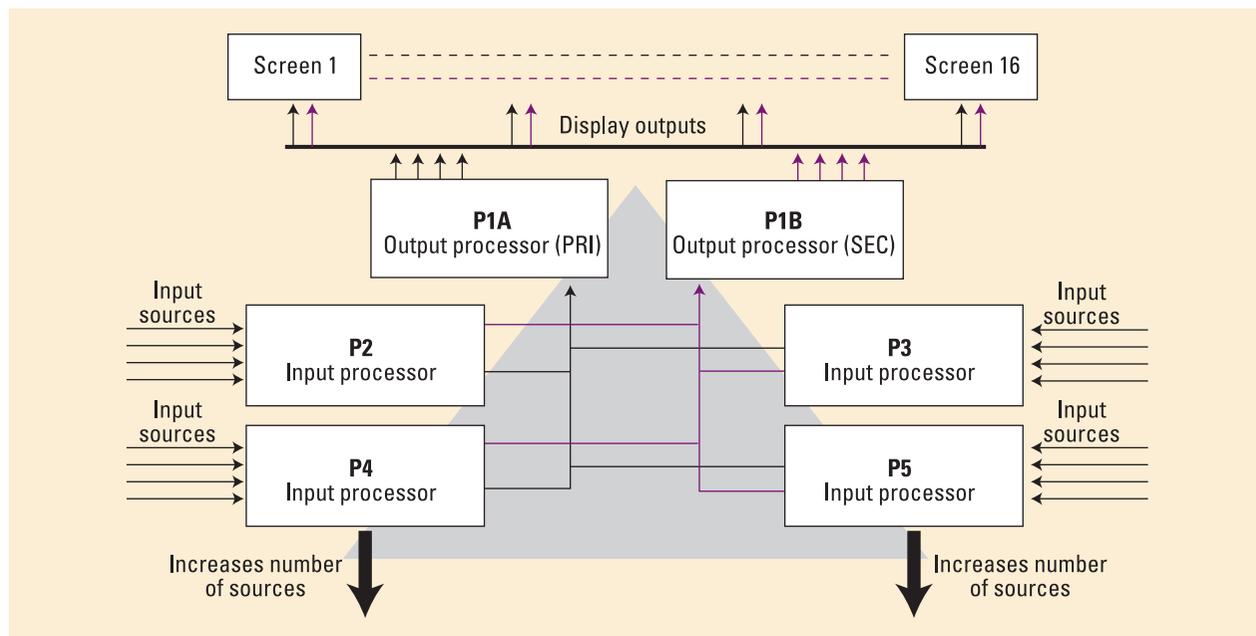


Figure 9. Cascaded architecture

put processors handling input sources only. If P2 becomes faulty, the only signals affected are sources connected to that frame. When additional input is required in the future, additional processor can be added to the tree.

The biggest drawback in this design is the limitation on the number of screens that can be driven. Most processors can only handle a maximum of 16 output screens. When signal sources have populated the screen with so many windows as the input expands, the visible images rendered become too small. It does not have the capability to expand the number of screens.

Summary

To effectively implement multi-image display monitoring, there are several technical baselines that must be

to know the canvas space a particular signal will require. Third, envision the common design canvas for all screens. Imagine how the picture will be presented per display (or forming arrays), including orientation. The next step is to choose deployment topology following the input formats, type, number of sources and screens, expansions, and reliability. Finally, choose the right multi-image display processor.

As supply of traditional CRT monitors continues to dry up, control rooms are turning toward implementing multi-image display to replace traditional monitoring. Fortunately, advances in display screen technology and use of high-speed FPGA in display processors allow presentation of stable and high quality images.

The key advantage of using multi-

ing and control workflow.

For instance, when a multi-image processor detects alarms and errors on its input, it can relay traps to the NMS manager about the faulty source. In turn, this can run routines to poll all connected devices to pinpoint defective component(s) along the chain. This gives the operators wide coverage of the system status plus visibility at quick glance.

BE

Augusto Villaseñor is a principle engineer with Globecomm Systems.

